FLORIDA ATLANTIC UNIVERSITY

NEW COURSE PROPOSAL
Undergraduate Programs

Department CEECS

College Engineering and Computer Science

*(To obtain a course number, contact **erudolph@fau.edu**)*

UUPC Approval _____
UFS Approval _____
SCNS Submittal _____
Confirmed _____
Banner Posted _____
Catalog _____

Prefix CDA

Number 4012C

(L = Lab Course; C = Combined Lecture/Lab; add if appropriate)

Lab Code C

Type of Course Lecture/Lab

Course Title Design of Digital Systems and Lab

Credits *(Review Provost Memorandum)* 3

Effective Date *(TERM & YEAR)* Spring 2021

Grading *(Select One Option)*

- **Regular** (●)
- **Pass/Fail** ( )
- **Sat/UnSat** ( )

Course Description *(Syllabus must be attached; Syllabus Checklist recommended; see Guidelines)*

In this course, students will learn to use a hardware description language (mainly VHDL) in the digital design process. Emphasis will be on system level concepts and high-level design representations. Students will also have the opportunity to use a commercial synthesis tool to automatically map high-level descriptions to Field Programmable Gate Arrays (FPGAs). The lab-intensive hands-on aspect of this course presents different approaches to the digital system modeling and design with the use of HDLs.

Prerequisites, with minimum grade*

CDA 3201C Introduction to Logic Design with minimum grade of "C"

Corequisites

NA

Registration Controls *(Major, College, Level)*

Default minimum passing grade is D-.** **Prereqs., Coreqs. & Reg. Controls are enforced for all sections of course

WAC/Gordon Rule Course

( ) **Yes** (●) **No**

WAC/Gordon Rule criteria must be indicated in syllabus and approval attached to proposal. See WAC Guidelines.

Intellectual Foundations Program (General Education) Requirement *(Select One Option)*

None

General Education criteria must be indicated in the syllabus and approval attached to the proposal. See GE Guidelines.

Minimum qualifications to teach course

PhD in CEECS

Faculty Contact/Email/Phone

razarderakhsh@fau.edu

List/Attach comments from departments affected by new course

Approved by		***Date***
Department Chair	Hanqi Zhuang (Digitally signed by Hanqi Zhuang, DN: cn=Hanqi Zhuang, o=FAU, ou=CEECS, email=zhuang@fau.edu, c=US, Date: 2020.06.04 13:58:45 -04'00')	6/4/2020
College Curriculum Chair	Dan Meeroff	9-3-20
College Dean		
UUPC Chair	Jerry Haky	9-15-20
Undergraduate Studies Dean	Edward Pratt	9-15-20
UFS President		
Provost		

Email this form and syllabus to mjenning@fau.edu seven business days before the UUPC meeting.

Department of Computer & Electrical Engineering
and Computer Science
Florida Atlantic University
Course Syllabus

1. Course title/number, number of credit hours	
CDA 4012C Design of Digital Systems and Lab	**3 credit hours (including lab)**
2. Course prerequisites, corequisites, and where the course fits in the program of study	
Prerequisites: CDA 3201C Introduction to Logic Design	
3. Course logistics	
Term: Spring 2021 This is a classroom lecture course which includes lab as well. *Class location and time* *Labs:*	
4. Instructor contact information	
Instructor's name *Office address* *Office Hours* *Contact telephone number* *Email address*	Reza Azarderakhsh EE314 W 3-4pm (or by appointment) (561) 297-4980 razarderakhsh@fau.edu
5. TA contact information	
TA's name *Office address* *Office Hours* *Contact telephone number* *Email address*	TBD
6. Course description	
In this course, students will learn to use a hardware description language (mainly VHDL) in the digital design process. Emphasis will be on system level concepts and high-level design representations. Students will also have the opportunity to use a commercial synthesis tool to automatically map high-level descriptions to Field Programmable Gate Arrays (FPGAs). The lab-intensive hands-on aspect of this course presents different approaches to the digital system modeling and design with the use of HDLs.	
7. Course objectives/student learning outcomes/program outcomes	
Course objectives	To learn hardware description language with hands-on experience on FPGA devices. To be skilled of register transfer level (RTL) design and gain knowledge of designing digital systems.
Student learning outcomes & relationship to ABET 1-7 outcomes	TBD
8. Course evaluation method	
Exam-I 25 % Homework 15 % Labs 30 % Exam-II 30 %	Exam II will not follow university final exams. It will be in or before last week of the class.
9. Course grading scale	

Grading Scale:
90 and above: "A",
87-89: "A-",
83-86: "B+",
80-82: "B",
77-79 : "B-",
73-76: "C+",
70-72: "C",
67-69: "C-",
63-66: "D+",
60-62: "D",
51-59: "D-",
50 and below: "F."

10. Policy on makeup tests, late work, and incompletes

Penalties for late submission will be 5% per day. Appropriate accommodations will be made for students having a valid medical excuse. Unless there exists an evidence of medical or emergency situation, incomplete grades will not be given. Plagiarism will not be tolerated. Any copying and pasting without attribution and a reference will be considered plagiarism.

11. Special course requirements

Each student will get and Nexys-4 DDR FPGA boards and will keep during the semester with no cost. The students need to return the board at the end of the semester. Any damages to the boards will be the students responsibility.

12. Classroom etiquette policy

University policy requires that in order to enhance and maintain a productive atmosphere for education, personal communication devices, such as cellular phones and laptops, are to be disabled in class sessions.

13. Attendance policy statement

Students are expected to attend all of their scheduled University classes and to satisfy all academic objectives as outlined by the instructor. The effect of absences upon grades is determined by the instructor, and the University reserves the right to deal at any time with individual cases of non-attendance.
Students are responsible for arranging to make up work missed because of legitimate class absence, such as illness, family emergencies, military obligation, court-imposed legal obligations or participation in University-approved activities. Examples of University-approved reasons for absences include participating on an athletic or scholastic team, musical and theatrical performances and debate activities. It is the student's responsibility to give the instructor notice prior to any anticipated absences and within a reasonable amount of time after an unanticipated absence, ordinarily by the next scheduled class meeting. Instructors must allow each student who is absent for a University-approved reason the opportunity to make up work missed without any reduction in the student's final course grade as a direct result of such absence.

14. Disability policy statement

In compliance with the Americans with Disabilities Act Amendments Act (ADAAA), students who require reasonable accommodations due to a disability to properly execute coursework must register with Student Accessibility Services (SAS) and follow all SAS procedures. SAS has offices across three of FAU's

campuses – Boca Raton, Davie and Jupiter – however disability services are available for students on all campuses. For more information, please visit the SAS website at www.fau.edu/sas/.

15. Counseling and Psychological Services (CAPS) Center

Life as a university student can be challenging physically, mentally and emotionally. Students who find stress negatively affecting their ability to achieve academic or personal goals may wish to consider utilizing FAU's Counseling and Psychological Services (CAPS) Center. CAPS provides FAU students a range of services – individual counseling, support meetings, and psychiatric services, to name a few – offered to help improve and maintain emotional well-being. For more information, go to http://www.fau.edu/counseling/

16. Code of Academic Integrity policy statement

Students at Florida Atlantic University are expected to maintain the highest ethical standards. Academic dishonesty is considered a serious breach of these ethical standards, because it interferes with the university mission to provide a high quality education in which no student enjoys an unfair advantage over any other. Academic dishonesty is also destructive of the university community, which is grounded in a system of mutual trust and places high value on personal integrity and individual responsibility. Harsh penalties are associated with academic dishonesty. For more information, see University Regulation 4.001. If your college has particular policies relating to cheating and plagiarism, state so here or provide a link to the full policy—but be sure the college policy does not conflict with the University Regulation.

17. Required texts/reading

To reduce costs for our students, we strongly encourage you to explore the adoption of open educational resources (OER), textbooks and other materials that are freely accessible. We also encourage you to clearly state in the syllabus if course materials are available on reserve in the Library.

Text: ***Fundamentals of Digital Logic with VHDL Design (3rd Edition)***, Stephen Brown and Zvonko Vranesic, ISBN 978-0-07-352953-0. (not mandatory course materials will be provides in the class.)

The book is available online. No need to purchase it.

18. Supplementary/recommended readings

- Pong P. Chu, RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability, Wiley-IEEE Press, 2014.

19. Course topical outline, including dates for exams/quizzes, papers, completion of reading

Weekly Schedule	Topics
Week 01	Review of Electronics Circuits Technology: MOS Transistor, CMOS logic
Week 02	VHDL-1 and Combinational/Sequential Logic Review
Week 3-4	VHDL- Behavioral modeling (Lab-1) Xilinx and Vivado Tools
Week 5-6	VHDL-Structural modeling Timing Analysis and simulation (Lab-2)
Week 7-8	VHDL-Dataflow modeling

Week 9	FPGA technology, Embedded resources, DSPs, memories, Slices, LUTs, FFs (Lab-3)
Week 10	VHDL-Test-benches (Lab-4)
Week 11	FSM/ASM design using VHDL (Lab-5)
Week 12	Testing of Digital Circuits
Week 13	Design for Testability and Self Testing Circuitry Functional (Lab-6)
Week 14	Performance Optimization: area, time, and power
Week 15	Verilog and Comparison with VHDL